PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: WAECHTER, D., et al.	Examiner: White, M.
Serial No.: Unknown	Art Unit: 2612
Filed: Herewith	
For: *READ-OUT CIRCUIT FOR ACTIVE MATRIX IMAGING ARRAYS*	
Date of Last Office Action: Not Applicable	
Attorney Docket No.: SMB 2 0719-2	

Cleveland, Ohio 44114
May 2, 2001

Assistant Commissioner For Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

Prior to calculation of the filing fee and examination of the above application, kindly enter the following amendments:

In the Specification:

On page 1, between lines 1 and 2 (i.e. after the Title and before Field of the Invention), please insert the following paragraph:

---**Cross Reference to Related Applications**

This application is a divisional of U.S. patent application Serial No. 08/930,749, filed December 2, 1997, now U.S. Patent No. _____, which claims priority from PCT/CA95/00202, filed on April 7, 1995.---

On page 8, the paragraph beginning on line 15 and ending on line 25 should be amended as follows:

Alternatives to the embodiments shown in Figures 2A and 2B are possible. For example, in Figure 2A the pixels are located to the right of pixels 1A and the number of source lines per pixel is reduced. However, this can be easily rearranged so that the pixels 1B are located beneath the pixels 1A as shown in Figure 2B, and reconfigured to increase the fill factor while still reducing the number of source lines per pixel. Likewise in Figure 3B, the pixels 1C are shown disposed to the right of the pixels 1A, and with dimensions selected to increase fill factor.

In the Claims:

Please cancel claims 1-34 that are presented in the International Publication No. W0/96/31976 (corresponding to International Application No. PCT/CA92/00202) that is submitted herewith. Said claims were canceled during international stage proceedings in favor of new claims 1-34 that are presented in the ANNEXES to the International Preliminary Examination Report Form (PCT/IPEA/409) that is also submitted herewith.

Please cancel claims 3-7 and 27 that are presented in the ANNEXES to the International Preliminary Examination Report Form (PCT/IPEA/409).

Please amend claims 23 and 24 that are presented in the ANNEXES to the International Preliminary Examination Report Form (PCT/IPEA/409) as follows:

23. (Amended) The improvement of claim 11, wherein each said thin-film-transistor (TFT) is a single gate device.

24. (Amended) The improvement of claim 11, wherein each said thin-film-transistor (TFT) is a dual gate device.

Please add new claims 35 and 36 as follows:

35. The improvement of claim 18, wherein each said thin-film-transistor (TFT) is a single gate device.

36. The improvement of claim 18, wherein each said thin-film-transistor (TFT) is a dual gate device.

REMARKS

Claims 3-7 and 27 as presented in Form (PCT/IPEA/409) have been canceled, claims 23 and 24 as presented in Form (PCT/IPEA/409) have been amended, and claims 35 and 36 have been added. Accordingly, claims 1, 2, 8-26, and 28-36 are presented for examination. Claims 23 and 24 were amended and claims 35 and 36 were added for the sole purpose of removing multiple claim dependencies, thus eliminating the filing fee surcharge that would otherwise have been necessary had the claims not been amended.

Entry of the foregoing amendments is respectfully requested.

Respectfully submitted,
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CERTIFICATE OF MAILING

I hereby certify that this PRELIMINARY AMENDMENT is being deposited with the United States Postal Service via EXPRESS MAIL in an envelope numbered EL852784359US and addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231, on May 2, 2001.

Georgeen B. George

Encl.: Version with Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

On page 8, the paragraph beginning on line 15 and ending on line 25 should be amended as follows:

Alternatives to the embodiments shown in Figures 2A and 2B are possible. For example, in Figure 2A the pixels are located to the right of pixels 1A and the number of source lines per [pwr] pixel is reduced. However, this can be easily rearranged so that the pixels 1B are located beneath the pixels 1A as shown in Figure 2B, and reconfigured to increase the fill factor while still reducing the number of source lines per pixel [so that the number of gate lines per pixel is reduced instead]. Likewise in Figure 3B, the pixels 1C are shown disposed to the right of the pixels 1A, and with dimensions selected to increase fill factor [thereby reducing the number of source lines per pixel, rather than the number of gate lines per pixel as in Figure 3A].

Please amend claims 23 and 24 that are presented in the ANNEXES to the International Preliminary Examination Report Form (PCT/IPEA/409) as follows:

23. (Amended) The improvement of claim [2,] 11, [or 18,] wherein each said thin-film-transistor (TFT) is a single gate device.

24. (Amended) The improvement of claim [2,] 11, [or 18,] wherein each said thin-film-transistor (TFT) is a dual gate device.